REMARKS

I. Status of the Application

Claims 1-19 are pending in this application. In the August 30, 2004 office action, the Examiner:

A. Required labeling of blocks of Fig. 2 of the drawing figures;

B. Rejected claim 13 under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 5,754,460 to Tam (hereinafter "Tam");

C. Rejected claim 1-19 under 35 U.S.C. § 112(b) as allegedly being indefinite; and

D. Deemed claims 1-12 and 14-19 allowable if rewritten or amended to overcome the indefiniteness rejections.

In this response, applicant has amended claims 1, 7, 8, 10, 11 and 19 to clarify the inventions claimed therein. Applicant has further canceled claims 5, 6 and 13-18. Applicant requests reconsideration and allowance of the claims 1-4, 7-12 and 19 in view of the foregoing amendments and the following remarks.

II. Figure 2 of the Drawings has been Amended

Applicant has submitted a replacement sheet which contains amendments to Fig. 2 of the drawings. The amendments conform to the Examiner's requirement that the blocks of the drawing figure be labeled. Applicants will submit a formal drawing upon acceptance by the Examiner.

III. The Indefiniteness Rejections are Moot

Claims 1-19 stand rejected as allegedly being indefinite. In particular, the Examiner noted specific issues with claims 1, 8, 10, 13, 14, 19. It is respectfully submitted that the alleged indefinite issues with claims 1, 8, 10, 13, 14 and 19 are now moot in view of the foregoing amendments.

In particular, with respect to claims 1, 14 and 19, the Examiner alleged that the claims were "mis-descriptive because the recited ANDing and ORing are not conditionally dependent on the sign of the first summation data value. . ." (August 30, 2004 office action at p. 2). Claim 14 has been canceled. Claims 1 and 19 have been amended to recite that the result of the ANDing and ORing operations are provided as output *conditional* on the sign of the first summation data value. It is respectfully submitted that such amendment renders the Examiner's issues with claims 1 and 19 moot. Claim 1 has other amendments relating to the rejection of claim 8, discussed below.

With respect to claim 8, the Examiner alleged that the multiplexer of the last three lines of claim 8 fail to fall within the scope of the second addition circuit as defined in claim 1. (*Id.*). Claim 1, prior to amendment, claimed that the addition circuit added a value one to the data value output of the shift circuit to form a second summation data value, depending on a sign of the first summation data value. Claim 8, which depended from claim 1, claimed that the addition circuit added the value one to the data value output, but only provided it as an output condition upon a control signal from a sign identification circuit.

It is respectfully submitted that claim 8 is not inconsistent with claim 1. The

second addition circuit of claim 1 conditions the *addition* of the value one to the shift circuit output data value upon *the sign of the first summation data value*. Claim 8 further recites that a multiplexer causes the output of the second addition circuit to either be the *added value* described above, or just the shift circuit data value output, depending on a control signal from the sign identification circuit. These claims are not inconsistent in that can be read to require different conditions for different results.

Nevertheless, claim 1 has been amended to clarify that the second summation circuit *provides an output* formed from the addition of the value one with the shift circuit output data value, but provides this output *dependent* on the sign of the first summation data value. Thus, instead of claiming the specific step of adding the value one to the output data value conditional upon the sign of the first summation data value, claim 1 merely states that such an added value is provided as an output depending on sign of the first summation data value. The amendment therefore leaves open the possibility that the added value is *only created* depending on the sign of the first summation data value, or that the added value is *only outputted* depending on the sign of the first summation data value.

Thus, claim 1 certainly allows, as claimed in claim 8, a second addition circuit that includes an adder and a multiplexer as claimed. In particular, claim 8 further specifies that an adder of the second summation circuit *adds* the value one to the shift circuit, and that a multiplexer of the second summation circuit determines whether this added value is passed on as the output. Thus, claim 8 is consistent with, although narrower than, claim 1 as amended. Because claims 1 and 8 are clearly consistent in wording, and would be clear to one of ordinary skill in the art, it is respectfully submitted

that the Examiner's issue with regard to claim 8 is moot.

With respect to claim 10, the Examiner alleged that the "multiplexer of the logic circuit" lacked a clear antecedent basis. Claim 10 has been amended such that the first instance of "multiplexer of the logic circuit" is preceded by the article "a". As a consequence, it is respectfully submitted that the Examiner's issue with regard to claim 10 is moot.

Claims 13 and 14 have been canceled without prejudice.

As a result, all of the issues with claims 1, 8, 10, 13, 14 and 19 raised by the Examiner in the indefiniteness rejection have been addressed. It is respectfully submitted that the indefiniteness rejection of the pending claims should be withdrawn.

IV. The Prior Art Objections are Moot

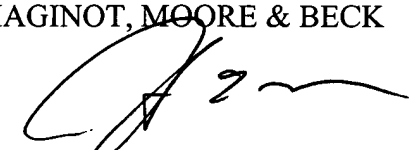
The Examiner rejected claim 13 as allegedly being anticipated. In the interest of expediency, claim 13 has been canceled, without prejudice. Such cancellation does not constitute an acquiescence in the Examiner's finding of anticipation.

V. Conclusion

For all of the foregoing reasons, it is respectfully submitted that the application is in a condition for allowance. Favorable reconsideration and allowance of this application is, therefore, earnestly solicited.

Respectfully Submitted,

MAGINOT, MOORE & BECK



January 31, 2005

Harold C. Moore
Registration No. 37,892
Bank One Center/Tower
111 Monument Circle, Suite 3000
Indianapolis, Indiana 46204-5115

Enclosures